

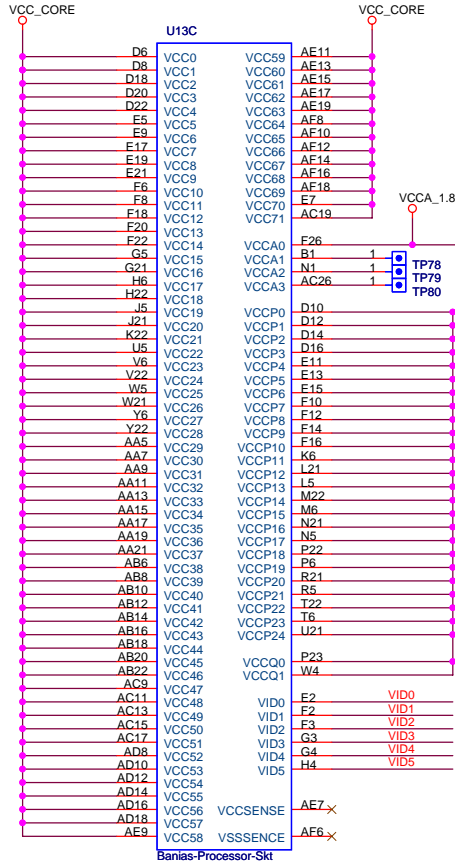
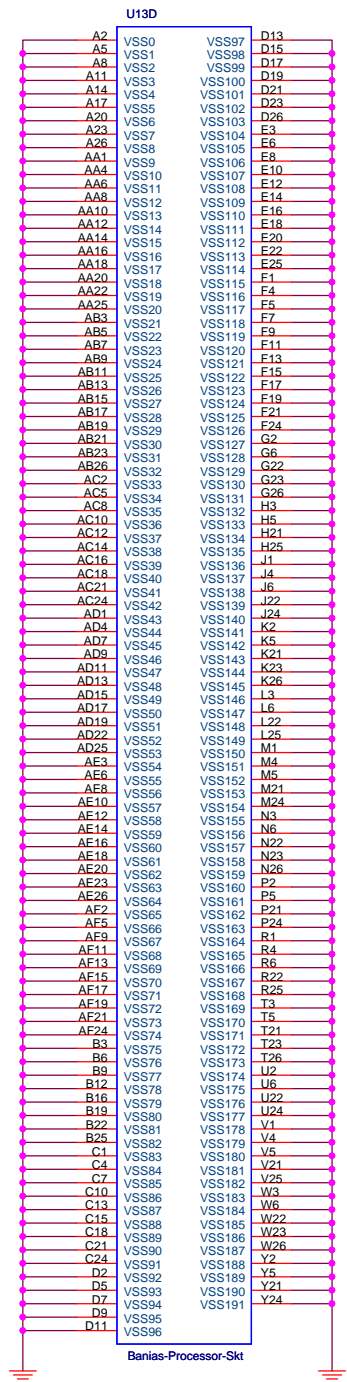
HISTORY
PAGE 31

PCB P/N:15-F63-011000

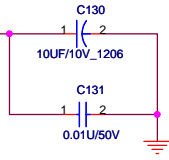
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DATE	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05
PAGE	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		
REV	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0					
DATE	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05	06/24/05					

Approved by	Checked by	Designed by
223 BLOCK DIAGRAM		
File	Document Number	Rev
	223-1-4-01	1.0
Date:	Friday, June 24, 2005	Sheet 1 of 32

P. Leader



0.01uf and 10uf of a pair capacitors



LAYOUT NOTE: Provide a test point (with no stub)
 LAYOUT NOTE: Provide a test point (with no stub)
 to connent differential probe between VCCSENSE
 and VSSSENSE at the location where the two 54.9
 ohm resistors terminate the 55 ohm transmission
 lines.

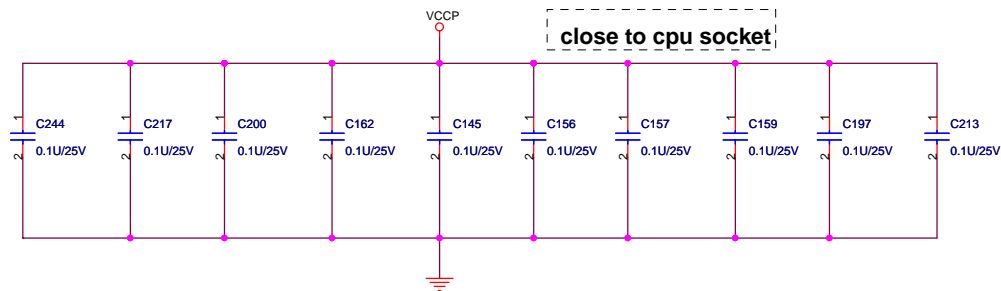
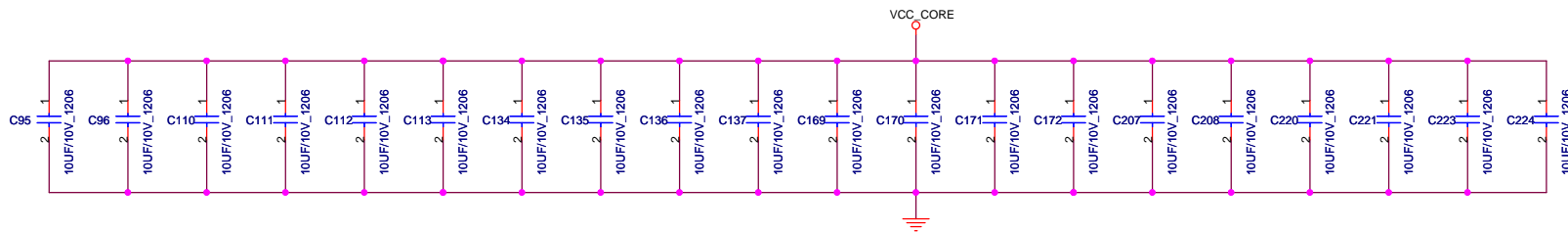
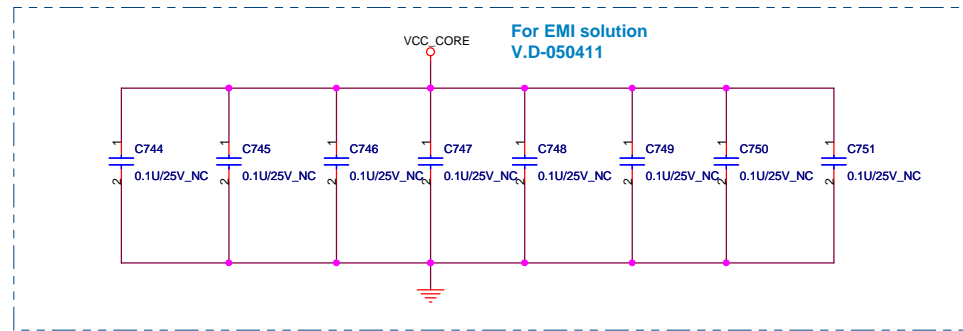
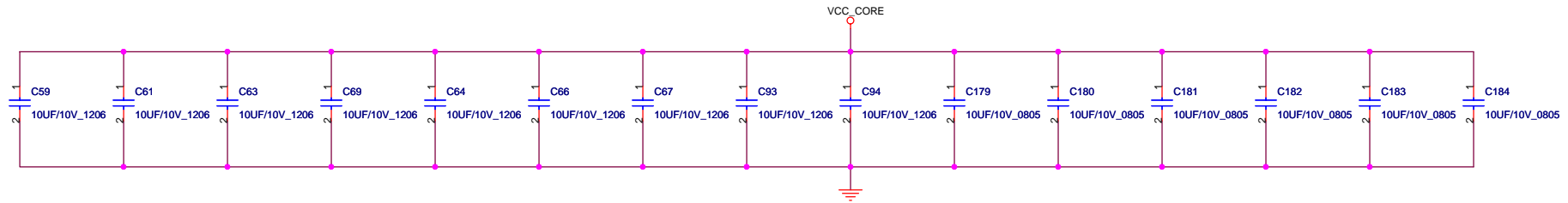


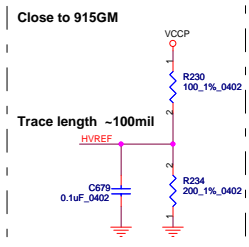
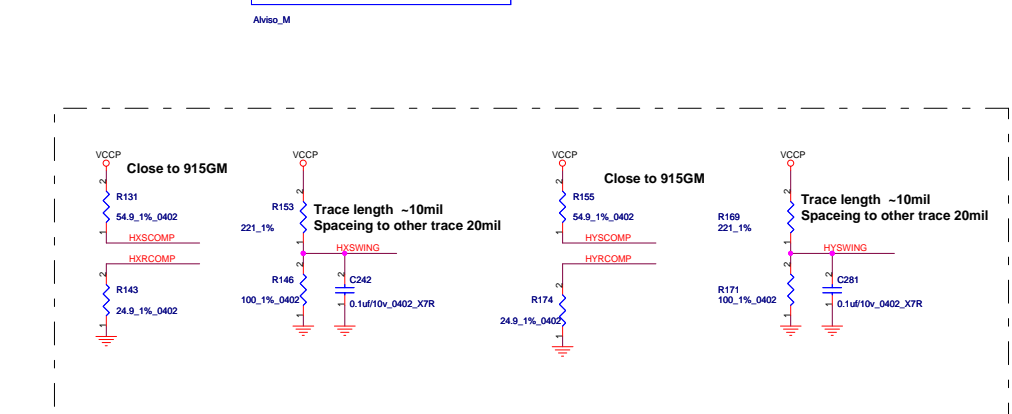
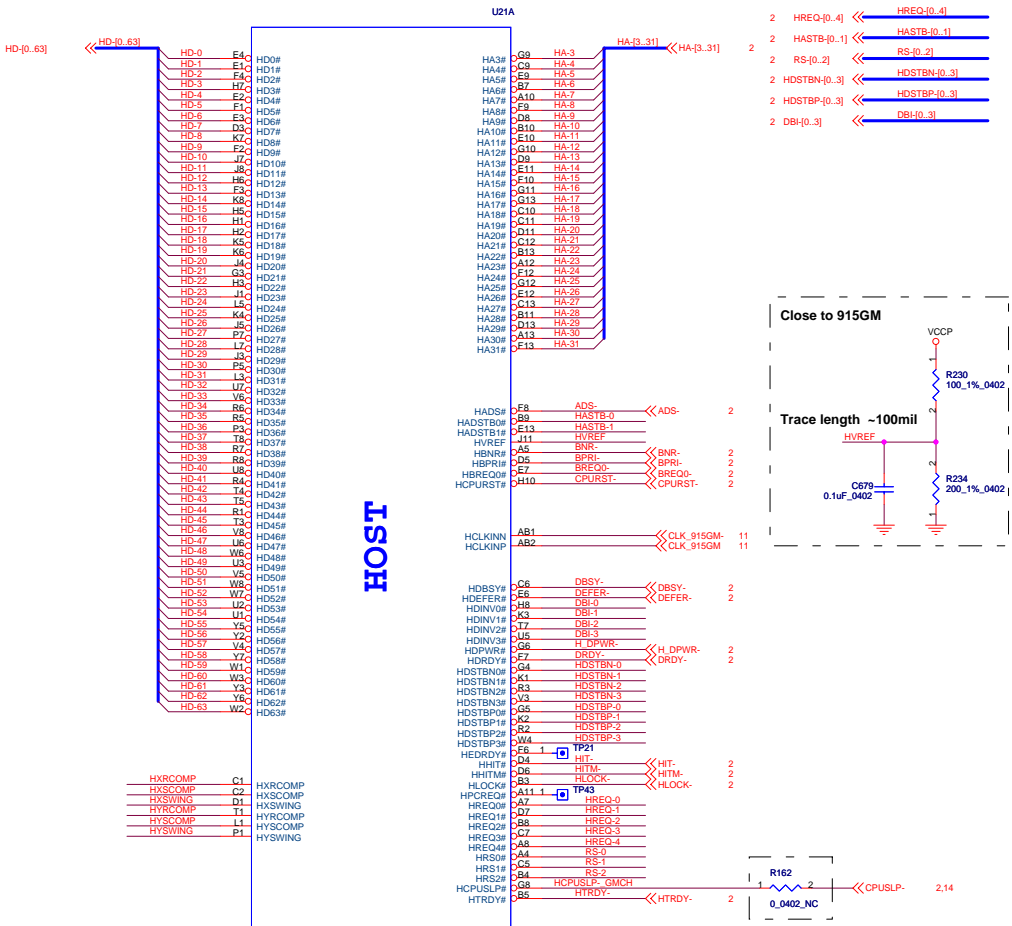
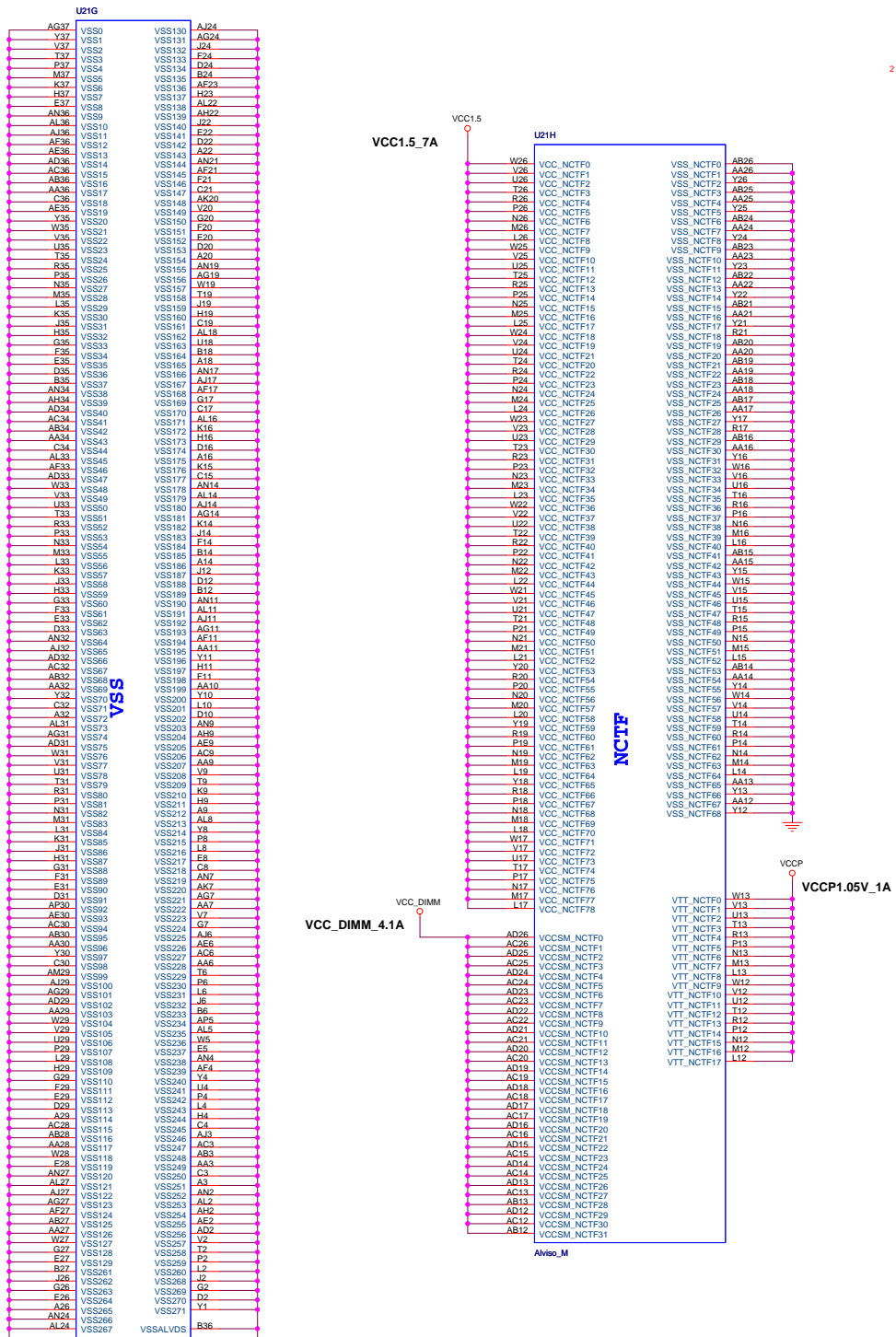
ECS Elitegroup Computer Systems

Title: **223 Dothan-2**

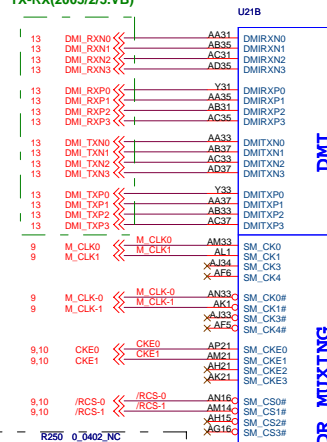
Size A3 Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 3 of 32

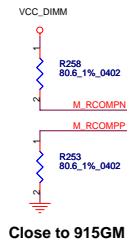




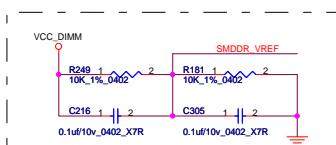
**CHANGR THE DMI BUS
TX-RX(2005/2/5.VB)**



Route as short as possible
DDR:Not used for DDR device.
Connect to GND.
DDR2:Pull down to GND with
40.2 ohm resistor.

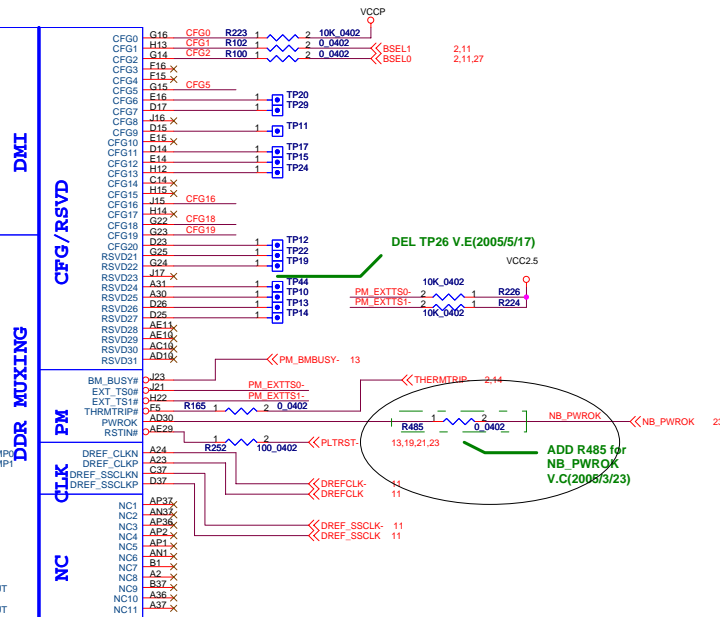


Close to 915GM



Close to 915GM

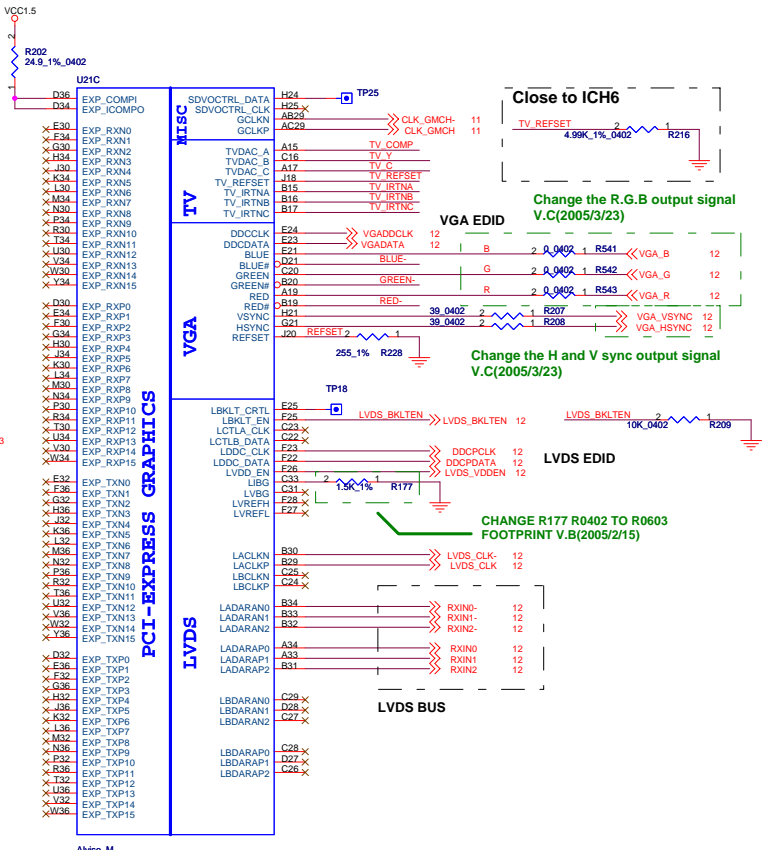
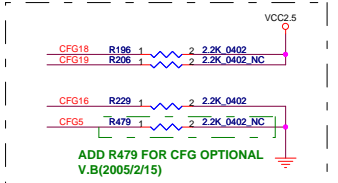
Aviso_M



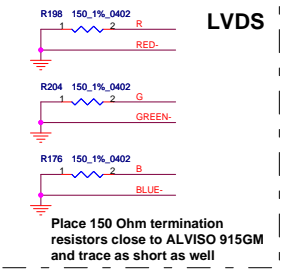
915GM CFG strapping

CFG[0..2] FSB Frequency Select
CFG[3..17] have internal pullup resistors
CFG[18..20] have internal pulldown resistors

CFG[2:0] 001= FSB 533 MHZ 101= FSB 400 MHZ	CFG16 0=Dynamic ODT Disable 1=Dynamic ODT Enable (default)
CFG5 0=DMix2 1=DMix4(default)	CFG11 0= CPU 533(default) NO FUNCTION NOW 1= CPU 400
CFG6 0=DDR2 1=DDR (default)	CFG18 0=1.05V(default) for 915PM 1=1.5V for 915GM Aviso 915GM core voltage select
CFG7 0=Mobile Prescott 1=Dothan (default)	CFG19 0= 1.05V(default) 1= 1.2V FSB I/O vlltage (CPU VTT select)
CFG9 0=Lane Reversal Enable 1=Normal Operation (default)	CFG13:12] 01=XOR MODE 10=All ZMODE 11=Normal Operation (Default)



DEL the 150 ohm ,connect the TV signal
to GND V.E(2005/5/18)



Place 150 Ohm termination
resistors close to ALVISO 915GM
and trace as short as well

/RMD[0:63] <<RMD[0:63] 9,10

/RDQS[0:7] <<RDQS[0:7] 9,10

/RDM[0:7] <<RDM[0:7] 9,10

MA DAT3 RP5A 8 1 10 8P4R 0402 /RMD3
MA DAT6 RP5B 7 2 10 8P4R 0402 /RMD6
MA DAT7 RP5C 6 3 10 8P4R 0402 /RMD2
MA DAT8 RP5D 5 4 10 8P4R 0402 /RMD15

MA DAT5 RP8A 8 1 10 8P4R 0402 /RMD5
MA DAT4 RP8B 7 2 10 8P4R 0402 /RMD4
MA DAT1 RP8C 6 3 10 8P4R 0402 /RMD1
MA DAT0 RP8D 5 4 10 8P4R 0402 /RMD0

MA DAT11 RP3A 8 1 10 8P4R 0402 /RMD11
MA DAT14 RP3B 7 2 10 8P4R 0402 /RMD14
MA DAT12 RP3C 6 3 10 8P4R 0402 /RMD17
MA DAT8 RP3D 5 4 10 8P4R 0402 /RMD8

MA DAT7 RP4A 8 1 10 8P4R 0402 /RMD7
MA DAT6 RP4B 7 2 10 8P4R 0402 /RMD9
MA DAT15 RP4C 6 3 10 8P4R 0402 /RMD15
MA DAT10 RP4D 5 4 10 8P4R 0402 /RMD10

MA DAT20 RP7A 8 1 10 8P4R 0402 /RMD20
MA DAT17 RP7B 7 2 10 8P4R 0402 /RMD17
MA DAT19 RP7C 6 3 10 8P4R 0402 /RMD19
MA DAT18 RP7D 5 4 10 8P4R 0402 /RMD19

MA DAT23 RP6A 8 1 10 8P4R 0402 /RMD23
MA DAT21 RP6B 7 2 10 8P4R 0402 /RMD21
MA DAT2 RP6C 6 3 10 8P4R 0402 /RMD22
MA DAT16 RP6D 5 4 10 8P4R 0402 /RMD16

MA DAT24 RP12A 8 1 10 8P4R 0402 /RMD24
MA DAT25 RP12B 7 2 10 8P4R 0402 /RMD25
MA DAT25 RP12C 6 3 10 8P4R 0402 /RMD25
MA DAT26 RP12D 5 4 10 8P4R 0402 /RMD26

MA DAT30 RP10A 8 1 10 8P4R 0402 /RMD30
MA DAT31 RP10B 7 2 10 8P4R 0402 /RMD31
MA DAT27 RP10C 6 3 10 8P4R 0402 /RMD27
MA DAT29 RP10D 5 4 10 8P4R 0402 /RMD29

MA DAT32 RP17A 8 1 10 8P4R 0402 /RMD32
MA DAT35 RP17B 7 2 10 8P4R 0402 /RMD33
MA DAT38 RP17C 6 3 10 8P4R 0402 /RMD38
MA DAT39 RP17D 5 4 10 8P4R 0402 /RMD39

MA DAT35 RP11A 8 1 10 8P4R 0402 /RMD35
MA DAT34 RP11B 7 2 10 8P4R 0402 /RMD34
MA DAT37 RP11C 6 3 10 8P4R 0402 /RMD37
MA DAT36 RP11D 5 4 10 8P4R 0402 /RMD36

MA DAT42 RP13A 8 1 10 8P4R 0402 /RMD42
MA DAT43 RP13B 7 2 10 8P4R 0402 /RMD43
MA DAT47 RP13C 6 3 10 8P4R 0402 /RMD47
MA DAT44 RP13D 5 4 10 8P4R 0402 /RMD44

MA DAT41 RP18A 8 1 10 8P4R 0402 /RMD45
MA DAT45 RP18B 7 2 10 8P4R 0402 /RMD47
MA DAT40 RP18C 6 3 10 8P4R 0402 /RMD40
MA DAT46 RP18D 5 4 10 8P4R 0402 /RMD46

MA DAT51 RP15A 8 1 10 8P4R 0402 /RMD51
MA DAT50 RP15B 7 2 10 8P4R 0402 /RMD50
MA DAT53 RP15C 6 3 10 8P4R 0402 /RMD53
MA DAT48 RP15D 5 4 10 8P4R 0402 /RMD48

MA DAT55 RP14A 8 1 10 8P4R 0402 /RMD55
M DOS6 RP14B 7 2 10 8P4R 0402 /RDQS6
MA DAT49 RP14C 6 3 10 8P4R 0402 /RMD49
MA DAT62 RP14D 5 4 10 8P4R 0402 /RMD62

M DOS7 RP16A 8 1 10 8P4R 0402 /RDQS7
MA DAT56 RP16B 7 2 10 8P4R 0402 /RMD56
MA DAT60 RP16C 6 3 10 8P4R 0402 /RMD60
MA DAT54 RP16D 5 4 10 8P4R 0402 /RMD54

MA DAT63 RP20A 8 1 10 8P4R 0402 /RMD63
MA DAT6 RP20B 7 2 10 8P4R 0402 /RMD62
M DM7 RP20C 6 3 10 8P4R 0402 /RDM7
MA DAT57 RP20D 5 4 10 8P4R 0402 /RMD57

MA DAT8 RP18A 8 1 10 8P4R 0402 /RMD8
M DM8 RP18B 7 2 10 8P4R 0402 /RDM8
MA DAT58 RP18C 6 3 10 8P4R 0402 /RMD58
MA DAT59 RP18D 5 4 10 8P4R 0402 /RMD59

/RDQS0 R28A 1 2 10 0402 M DOS0
/RDQS1 R31A 1 2 10 0402 M DOS1
/RDQS2 R36 1 2 10 0402 M DOS2
/RDQS3 R31 1 2 10 0402 M DOS3
/RDQS4 R36 1 2 10 0402 M DOS4
/RDQS5 R32 1 2 10 0402 M DOS5

/RDM0 R310 1 2 10 0402 M DM0
/RDM1 R315 1 2 10 0402 M DM1
/RDM2 R297 1 2 10 0402 M DM2
/RDM3 R285 1 2 10 0402 M DM3
/RDM4 R286 1 2 10 0402 M DM4
/RDM5 R329 1 2 10 0402 M DM5

U21D

MA DAT0	AG35	SADD0	SA_BS0F	AK15	M_BS0	9,10
MA DAT1	AH35	SADD1	SA_BS0F	AK16	M_BS1	9,10
MA DAT2	AL35	SADD2	SA_BS2F	AK15		
MA DAT3	AL37	SADD3				
MA DAT4	AH36	SADD3				
MA DAT5	AJ35	SADD5	SA_DM0	AJ37	M_DM0	
MA DAT7	AL34	SADD6	SA_DM1	AP35	M_DM1	
MA DAT8	AN35	SADD7	SA_DM2	AP29	M_DM2	
MA DAT10	AP32	SADD9	SA_DM3	AP24	M_DM3	
MA DAT11	AM31	SADD10	SA_DM4	AP4	M_DM5	
MA DAT12	AM34	SADD11	SA_DM6	AP3	M_DM6	
MA DAT13	AM35	SADD12	SA_DM7	AD3	M_DM7	
MA DAT16	AL32	SADD14				
MA DAT17	AN31	SADD15				
MA DAT18	AN32	SADD16				
MA DAT19	AN38	SADD18	SA_DQ0D	AK36	M_DQ0D	
MA DAT19	AP28	SADD19	SA_DQ1S	AK29	M_DQ1S	
MA DAT20	AL30	SADD20	SA_DQ3S	AP23	M_DQ3S	
MA DAT21	AM30	SADD21	SA_DQ3A	AM6	M_DQ3A	
MA DAT22	AM28	SADD22	SA_DQ3B	AM4	M_DQ3B	
MA DAT23	AL28	SADD23	SA_DQ3E	AJ1	M_DQ3E	
MA DAT24	AP27	SADD23	SA_DQ3F	AE5	M_DQ3F	
MA DAT25	AM27	SADD25				
MA DAT26	AM23	SADD26	SA_DQ5F	AK35	M_DQ5F	
MA DAT27	AM22	SADD26	SA_DQ5B	CAN34		
MA DAT28	AL23	SADD28	SA_DQ5C	CAN30		
MA DAT29	AM24	SADD29	SA_DQ5D	CAN8		
MA DAT30	AN22	SADD30	SA_DQ5E	CAN5		
MA DAT31	AP22	SADD31	SA_DQ5F	CAN3		
MA DAT32	AM9	SADD32	SA_DQ5F	AH15		
MA DAT33	AL9	SADD32	SA_DQ5F	AH15		
MA DAT34	AL6	SADD33				
MA DAT35	AP7	SADD34				
MA DAT36	AP11	SADD35	SA_MA0	AL17	M_A0	
MA DAT37	AP10	SADD36	SA_MA1	AP17	M_A1	
MA DAT38	AL7	SADD37	SA_MA2	AP18	M_A2	
MA DAT39	AM7	SADD38	SA_MA3	AM17	M_A3	
MA DAT40	AN6	SADD40	SA_MA4	AN18	M_A4	
MA DAT41	AN6	SADD41	SA_MA5	AM18	M_A5	
MA DAT42	AN3	SADD42	SA_MA6	AL19	M_A6	
MA DAT43	AP4	SADD43	SA_MA7	AP20	M_A7	
MA DAT44	AP6	SADD44	SA_MA8	AM19	M_A8	
MA DAT45	AM6	SADD45	SA_MA9	AL20	M_A9	
MA DAT46	AL4	SADD46	SA_MA10	AM16	M_A10	
MA DAT47	AK3	SADD48	SA_MA11	AM20	M_A11	
MA DAT48	AK2	SADD48	SA_MA12	AM20	M_A12	
MA DAT49	AK3	SADD49	SA_MA13	AM15	M_A13	
MA DAT50	AG2	SADD50				
MA DAT51	AG1	SADD51				
MA DAT52	AL3	SADD52				
MA DAT53	AM2	SADD52				
MA DAT54	AH3	SADD54				
MA DAT55	AG3	SADD54				
MA DAT56	AF3	SADD55				
MA DAT57	AE3	SADD57	SA_CAS#	CAN15	M_CAS#	9,10
MA DAT58	AD6	SADD58	SA_RAS#	CAP16	M_RAS#	9,10
MA DAT59	AC4	SADD58	SA_RCVENOUT#	CAE29		
MA DAT60	AF2	SADD60	SA_WE#	CAE28		
MA DAT61	AF1	SADD61				
MA DAT62	AD4	SADD61				
MA DAT63	AD5	SADD62				
		SADD63				

DDR SYSTEM MEMORY A

Alviso_M

U21E

SA_BS0F	AK15	M_BS0	9,10
SA_BS2F	AK16	M_BS1	9,10
SA_BS2F	AK15		
SA_DM0	AJ37	M_DM0	
SA_DM1	AP35	M_DM1	
SA_DM2	AP29	M_DM2	
SA_DM3	AP24	M_DM3	
SA_DM4	AP4	M_DM5	
SA_DM6	AP3	M_DM6	
SA_DM7	AD3	M_DM7	
SA_DQ0D	AK36	M_DQ0D	
SA_DQ1S	AK29	M_DQ1S	
SA_DQ3S	AP23	M_DQ3S	
SA_DQ3A	AM6	M_DQ3A	
SA_DQ3B	AM4	M_DQ3B	
SA_DQ3E	AJ1	M_DQ3E	
SA_DQ3F	AE5	M_DQ3F	
SA_DQ5F	AK35	M_DQ5F	
SA_DQ5B	CAN34		
SA_DQ5C	CAN30		
SA_DQ5D	CAN8		
SA_DQ5E	CAN5		
SA_DQ5F	CAN3		
SA_DQ5F	AH15		
SA_DQ5F	AH15		
SA_MA0	AL17	M_A0	
SA_MA1	AP17	M_A1	
SA_MA2	AP18	M_A2	
SA_MA3	AM17	M_A3	
SA_MA4	AN18	M_A4	
SA_MA5	AM18	M_A5	
SA_MA6	AL19	M_A6	
SA_MA7	AP20	M_A7	
SA_MA8	AM19	M_A8	
SA_MA9	AL20	M_A9	
SA_MA10	AM16	M_A10	
SA_MA11	AM20	M_A11	
SA_MA12	AM20	M_A12	
SA_MA13	AM15	M_A13	
SA_CAS#	CAN15	M_CAS#	9,10
SA_RAS#	CAP16	M_RAS#	9,10
SA_RCVENOUT#	CAE29		
SA_WE#	CAE28		
	CAE15	M_WE#	9,10

DDR SYSTEM MEMORY B

Alviso_M

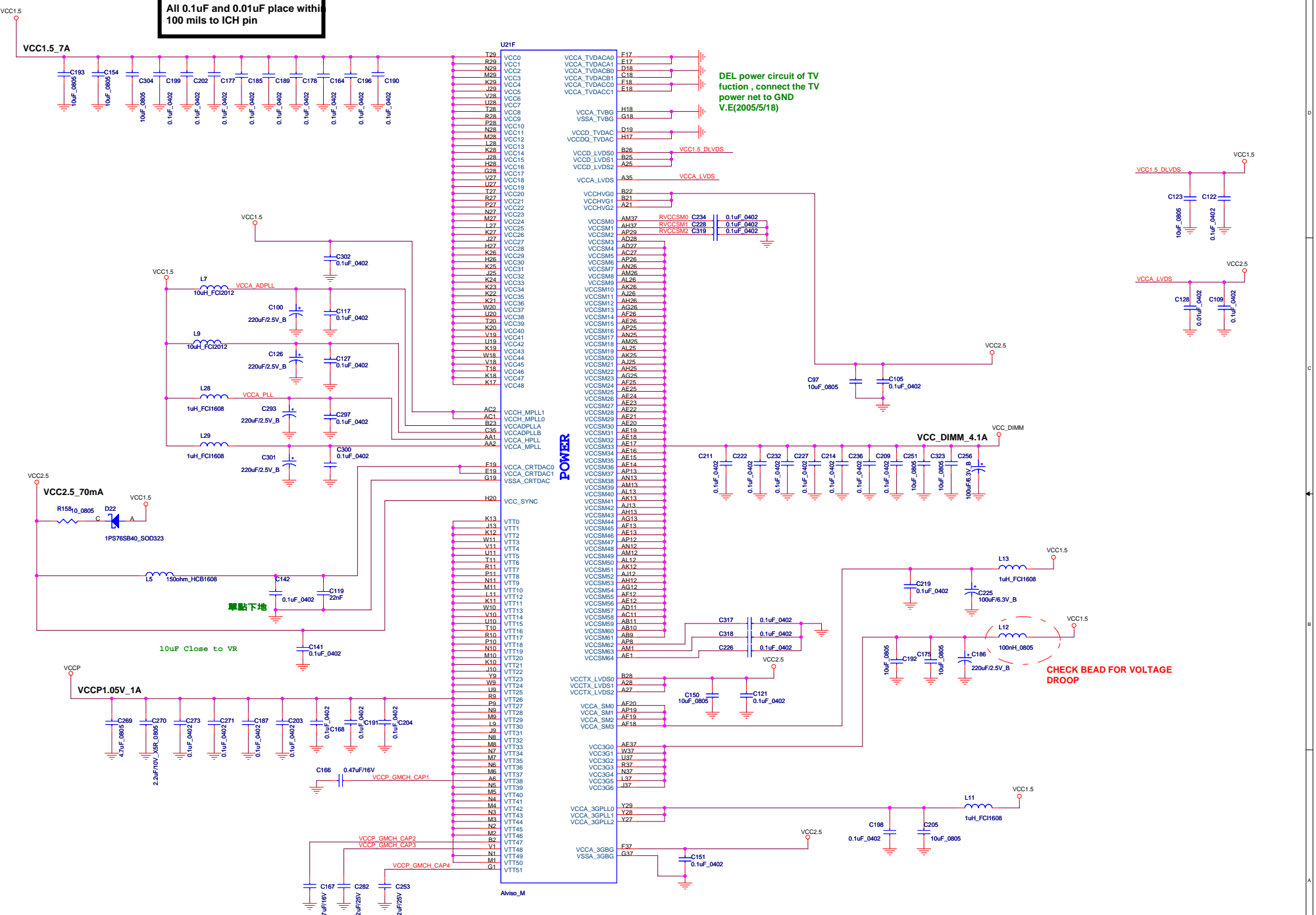
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Title: **223 ALVISO_C (DDR)**

Size C Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 7 of 32

All 0.1uF and 0.01uF place with 100 mils to ICH pin



7,10 M_A[0..13] >> M_A[0..13]
 6,10 CKE[0:1] >> CKE[0:1]
 7,10 /RDM[0..7] >> /RDM[0..7]
 7,10 /RDQS[0..7] >> /RDQS[0..7]

M_A0 112 A0
 M_A1 111 A1
 M_A2 110 A2
 M_A3 109 A3
 M_A4 108 A4
 M_A5 107 A5
 M_A6 106 A6
 M_A7 105 A7
 M_A8 102 A8
 M_A9 101 A9
 M_A10 115 A10/AP
 M_A11 100 A11
 M_A12 99 A12
 M_A13 97 DU/A13

M_BS0 117 BA0
 M_BS1 116 BA1
 X 98 DU/BA2

/RCS-0 121 CS0
 /RCS-1 122 CS1

/RDM0 12 DQM0
 /RDM1 26 DQM1
 /RDM2 48 DQM2
 /RDM3 62 DQM3
 /RDM4 134 DQM4
 /RDM5 148 DQM5
 /RDM6 170 DQM6
 /RDM7 184 DQM7
 X 78 DQM8

M_WE- 119 WE
 M_CAS- 120 CAS
 M_RAS- 118 RAS

CKE0 96 CKE0
 CKE1 95 CKE1

M_CLK0 35 CK0
 M_CLK-0 37 CK0
 M_CLK1 160 CK1
 M_CLK-1 158 CK1
 X 89 CK2
 X 91 CK2

/RDQS0 11 DQS0
 /RDQS1 25 DQS1
 /RDQS2 47 DQS2
 /RDQS3 61 DQS3
 /RDQS4 133 DQS4
 /RDQS5 147 DQS5
 /RDQS6 169 DQS6
 /RDQS7 183 DQS7
 X 77 DQS8

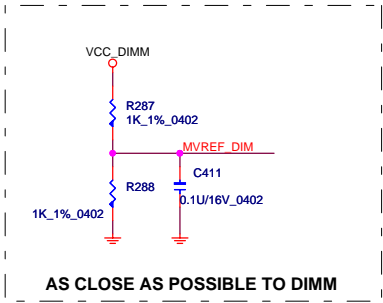
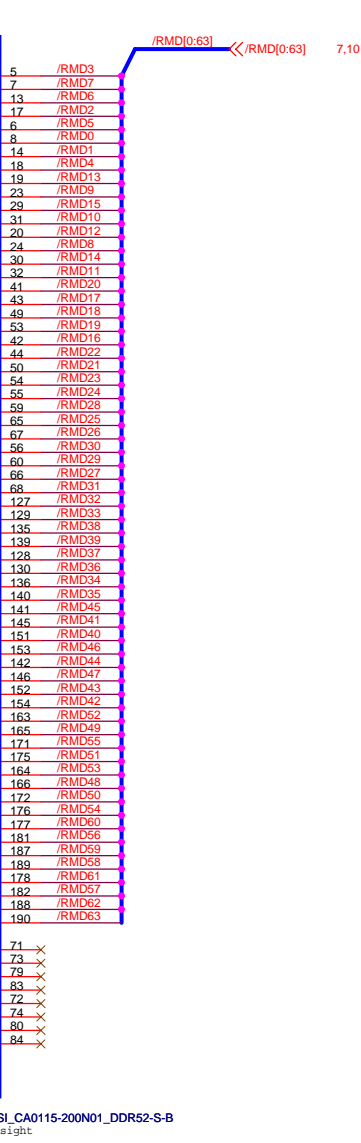
SMBDATA 193 SDA
 SMBCLK 195 SCL

SA0 194
 SA1 196
 SA2 198

VREF1 197
 VREF2 199

VDDID 197
 VDDSPD 199

NC/DU/RESET 86
 NC/DU1 85
 NC/DU2 123
 NC/DU3 124
 NC/DU4 200



STANDARD

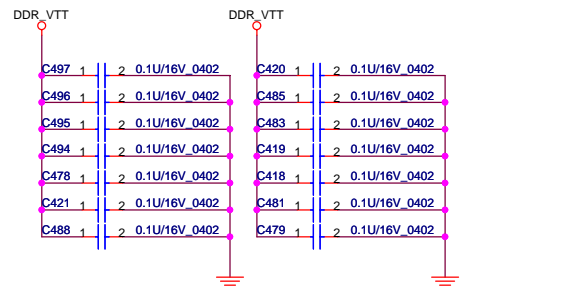
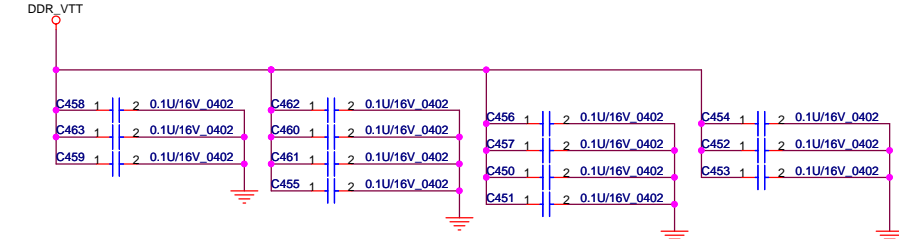
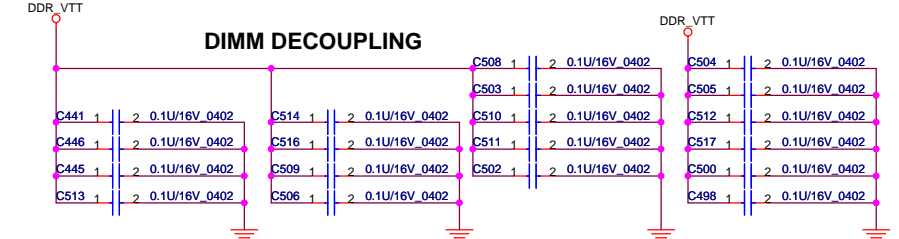
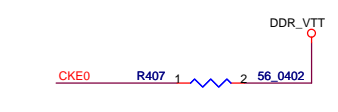
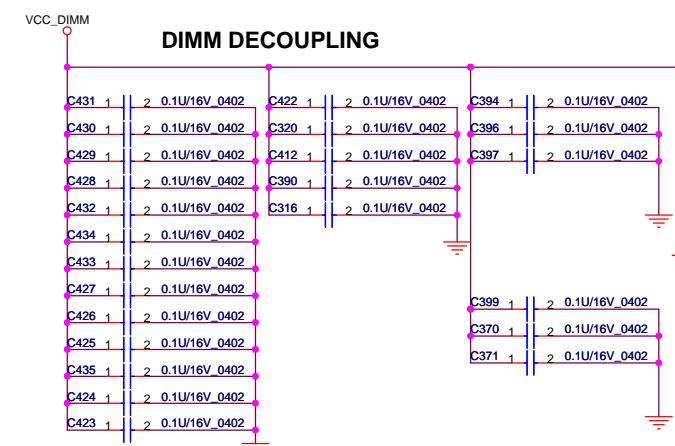
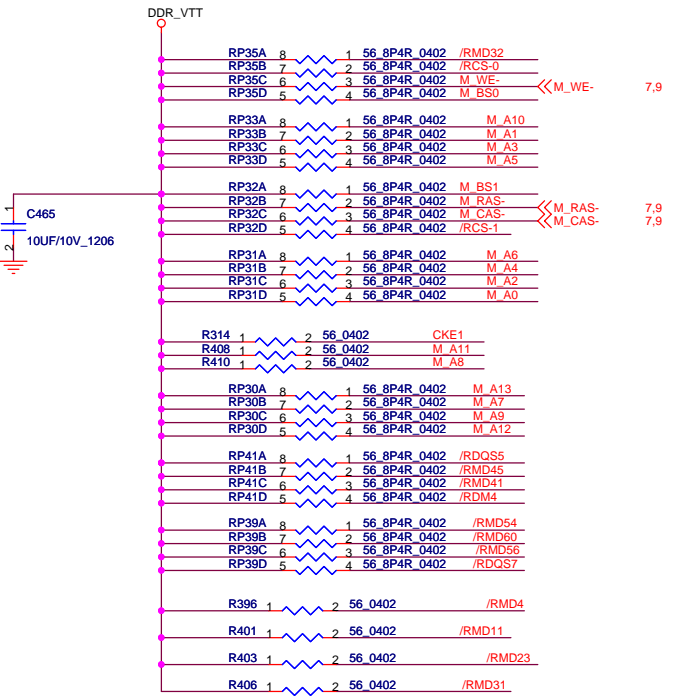
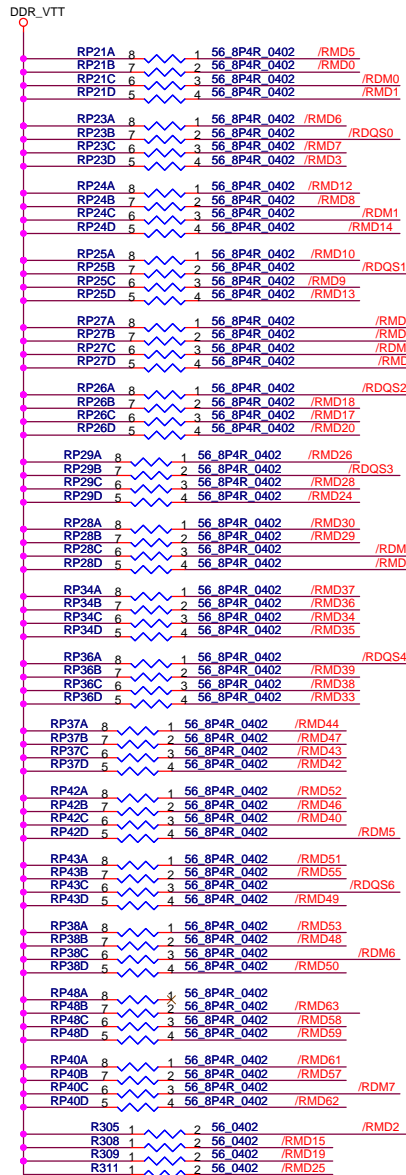
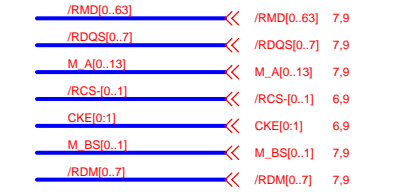
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Title: **223 DDR SODIMM**

Size A3 Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 9 of 32

DDR Parallel Termination



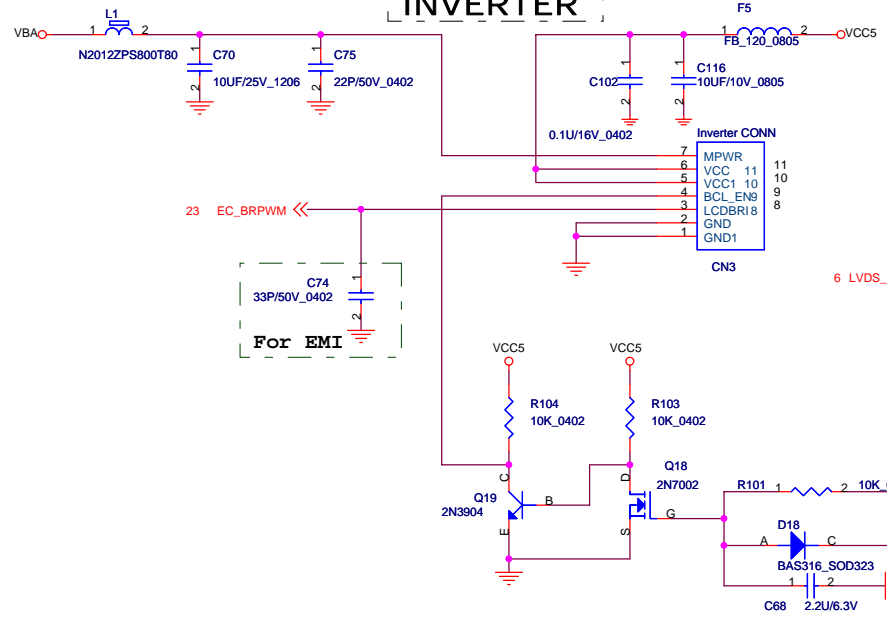
Elitegroup Computer Systems

Title: **223 DDR Termination**

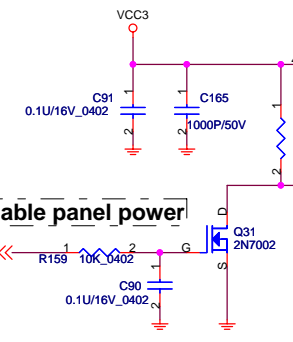
Size A3 | Document Number: **223-1-4-01** | Rev 1.0

Date: Friday, June 24, 2005 | Sheet 10 of 32

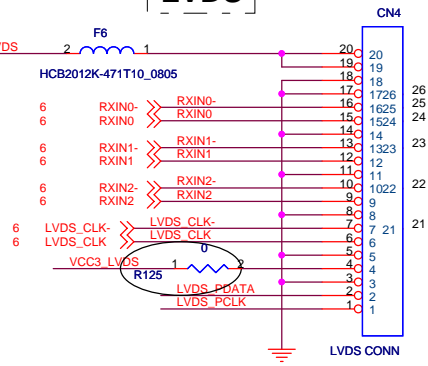
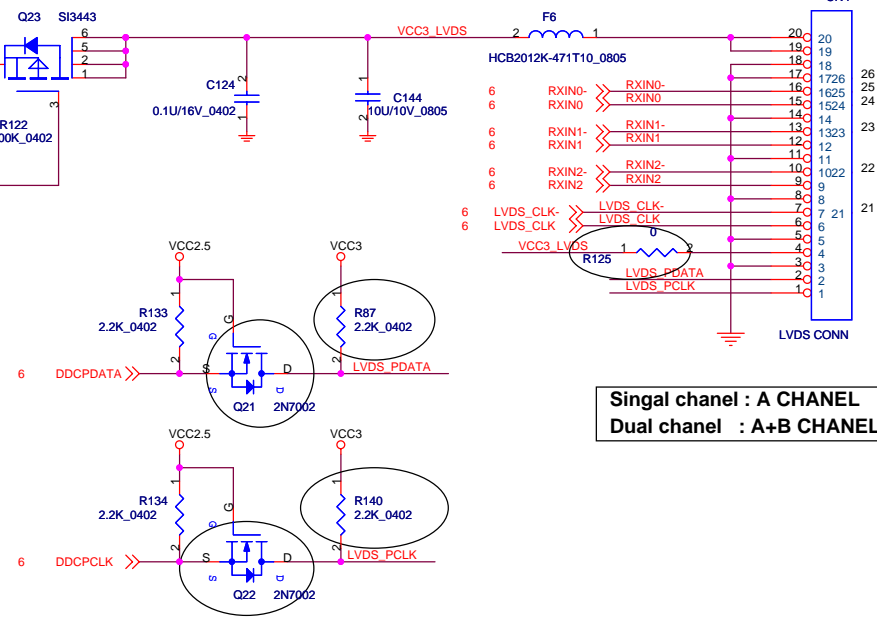
INVERTER



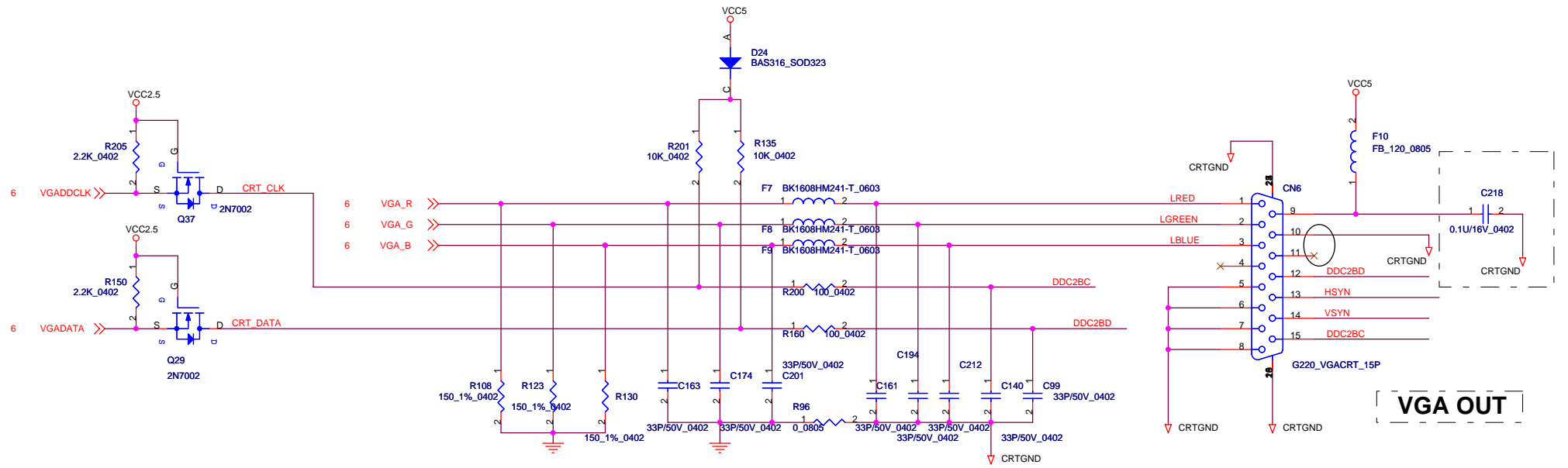
Enable panel power



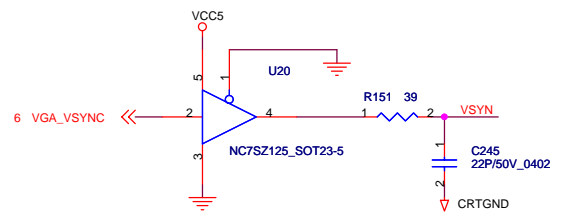
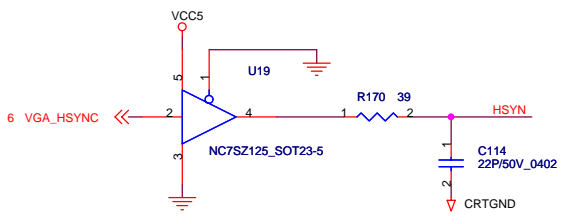
LVDS



Signal channel : A CHANEL
Dual channel : A+B CHANEL



VGA OUT

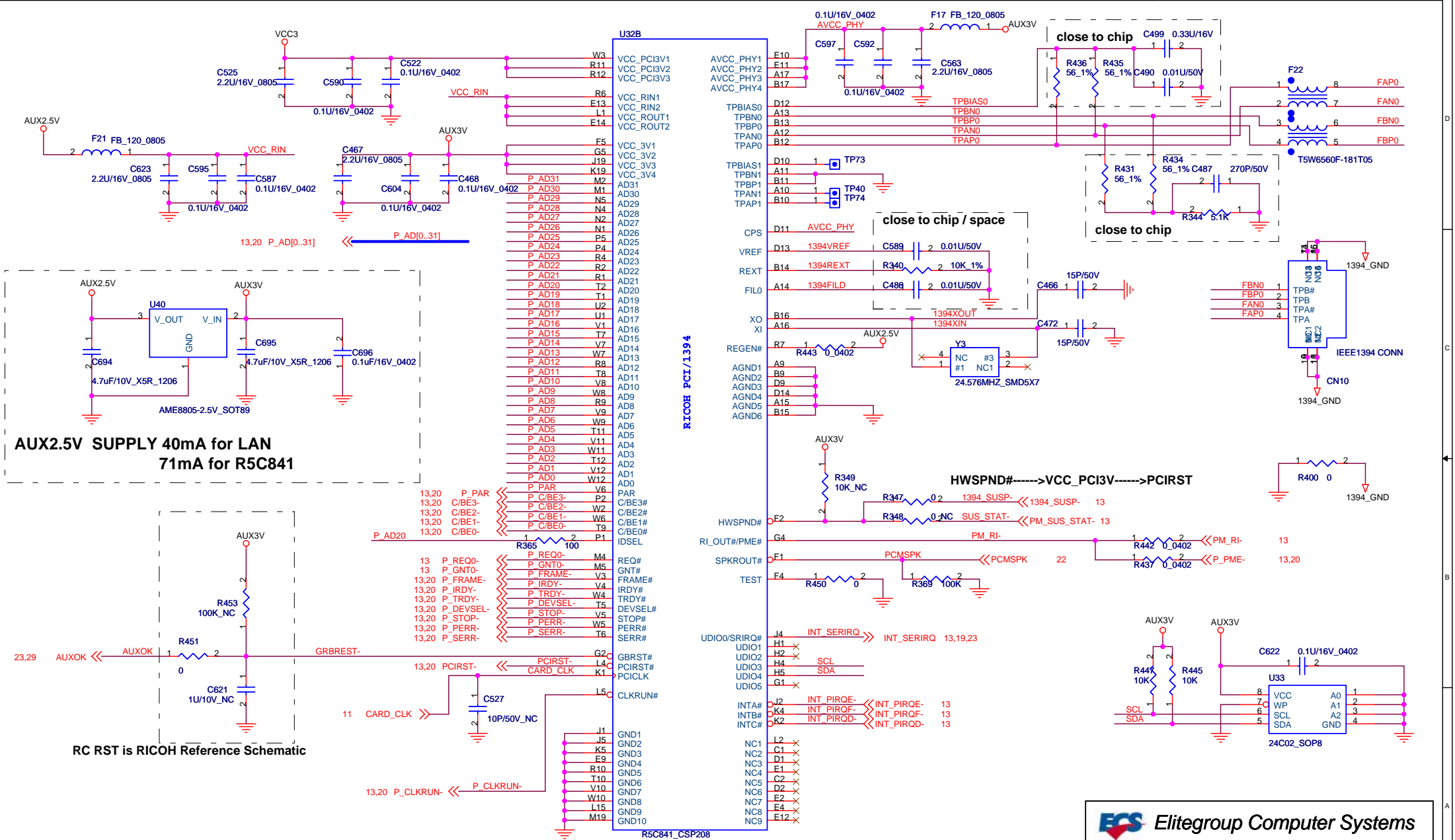


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Title: **223 LVDS & CRT**

Size A3 Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 12 of 32



**AUX2.5V SUPPLY 40mA for LAN
71mA for R5C841**

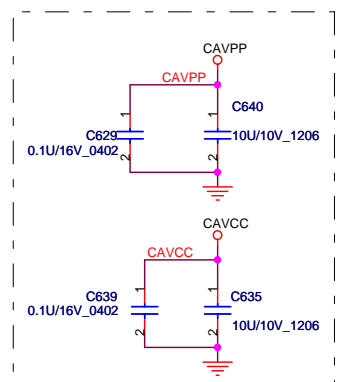
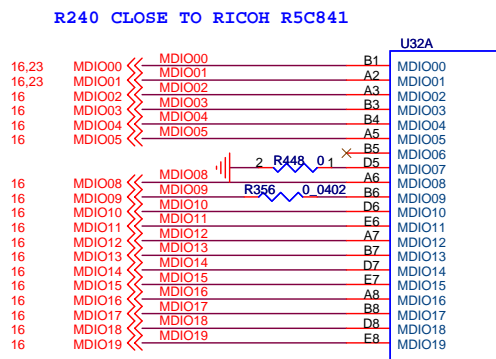
RC RST is RICOH Reference Schematic

ECS Elitegroup Computer Systems

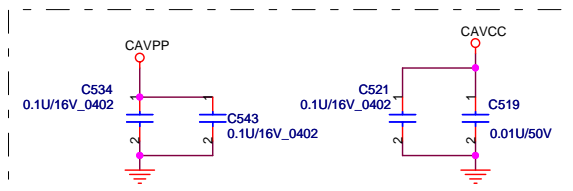
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Size B Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 17 of 32

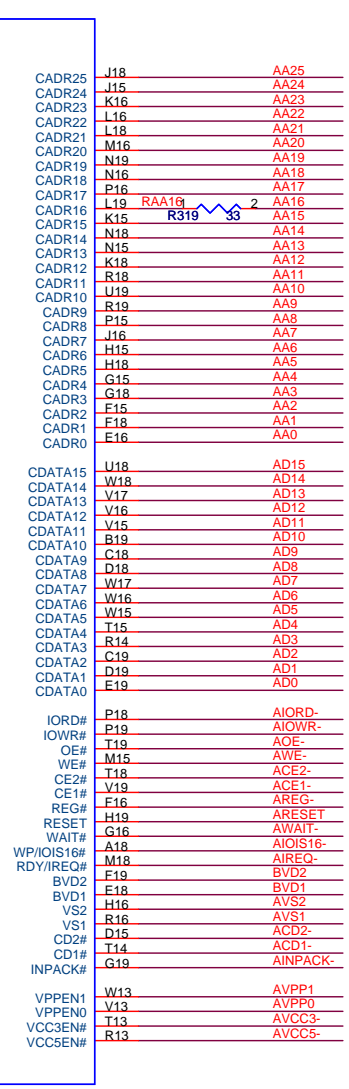


Close to R5C841

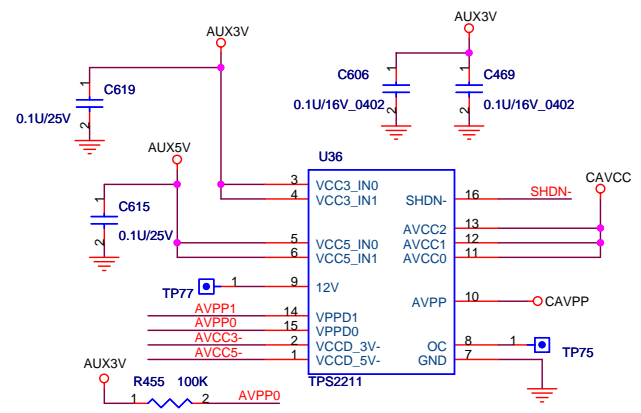


Close to CN13

RICOH CARBUS/CARDREADER



AA16 is critical signal
R241 close to chip



ADD SHDN- PULL UP resistor V.C(2005/3/11)

CAVPP OUTPUT STATE

AVPPD0	AVPPD1	OUTPUT
H	L	CAVPP(12V)
L	H	AVCC

CAVCC OUTPUT STATE

AVCC5-	AVCC3-	OUTPUT
H	L	3.3V
L	H	5V

ECS Elitegroup Computer Systems

Title: **223 R5C841 CARBUS/CARDREADER**

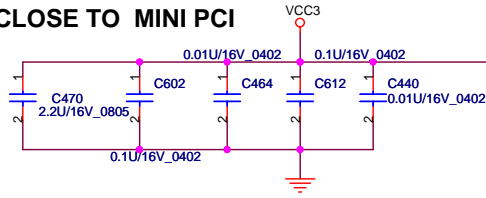
Size B Document Number: **223-1-4-01** Rev 1.0

Date: Friday, June 24, 2005 Sheet 18 of 32

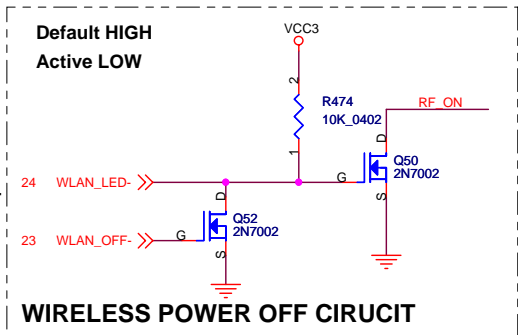
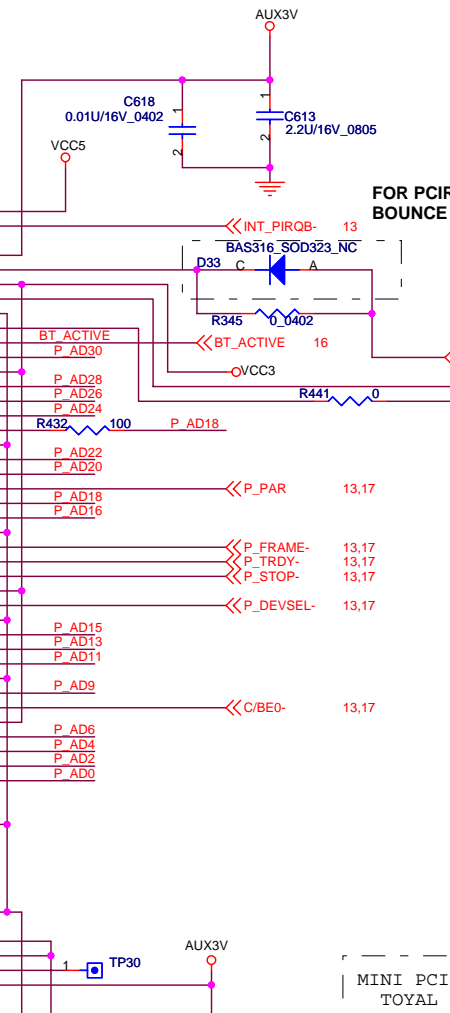
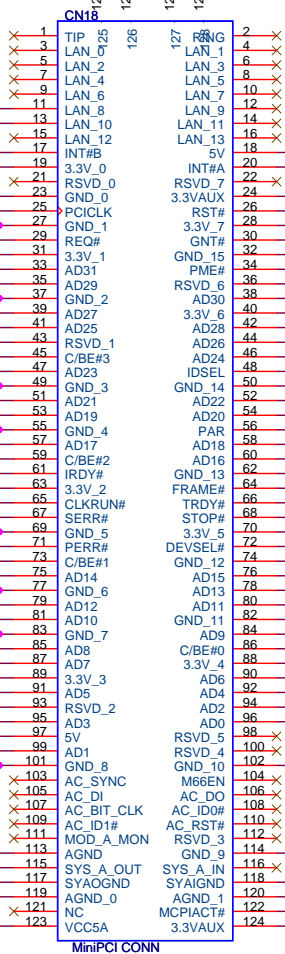
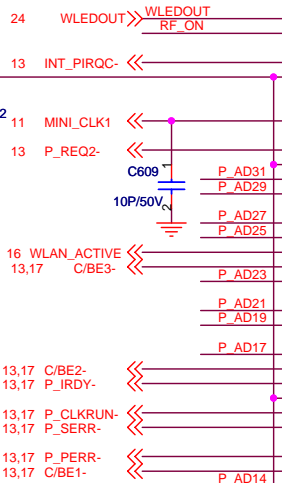
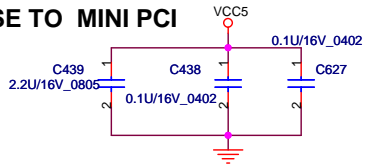
P_AD0..31 << P_AD0..31 13,17

MINI PCI SOCKET

CLOSE TO MINI PCI



CLOSE TO MINI PCI



MINI PCI POWER SPEC.
 TOYAL : 2W
 +5V : 100mA
 3.3VAUX : 5/200/375mA
 VCC5A : 100mA
 +3V

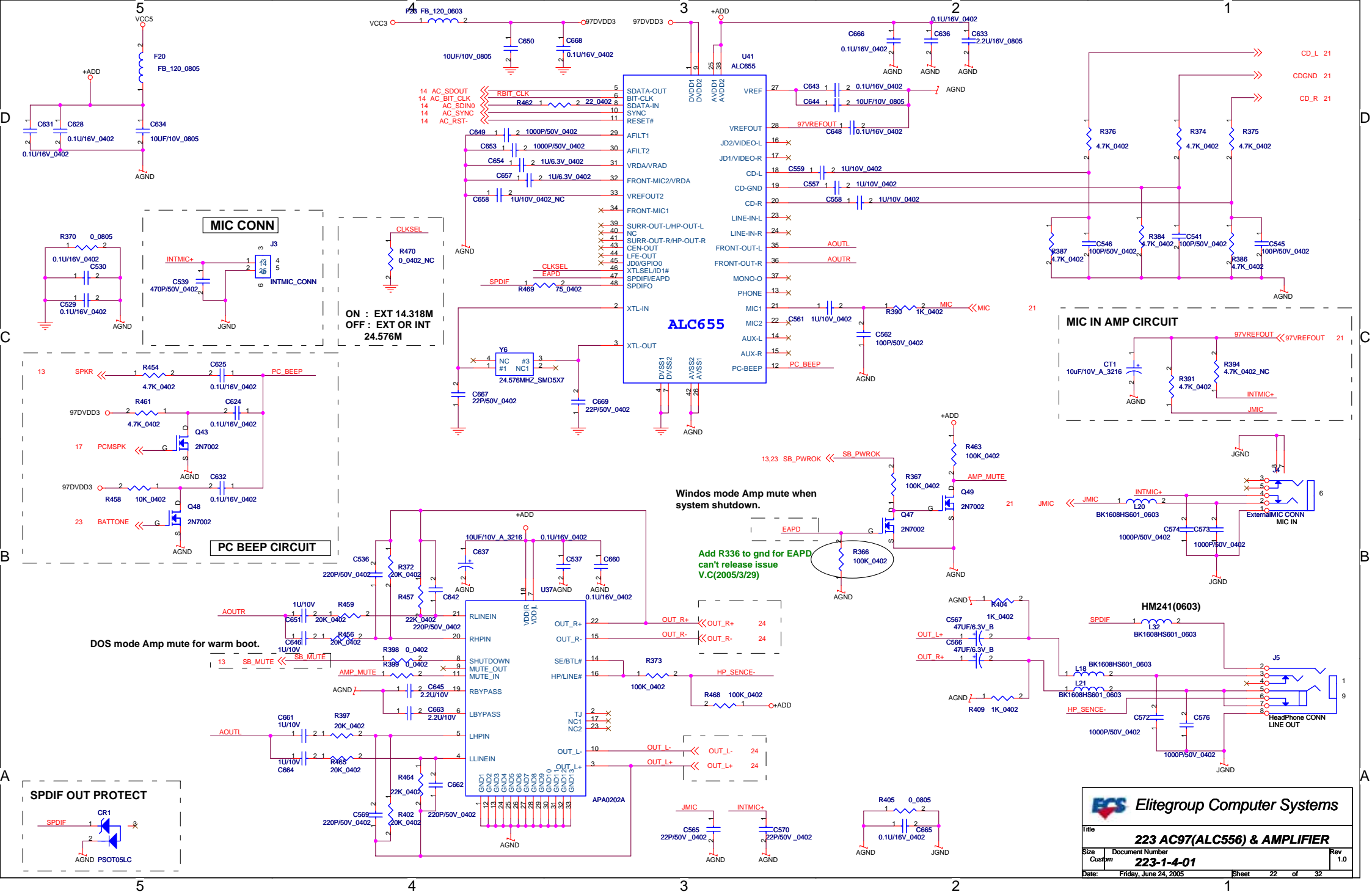
FOR G223 :
 PHONE AND MONO_OUT NOT USE

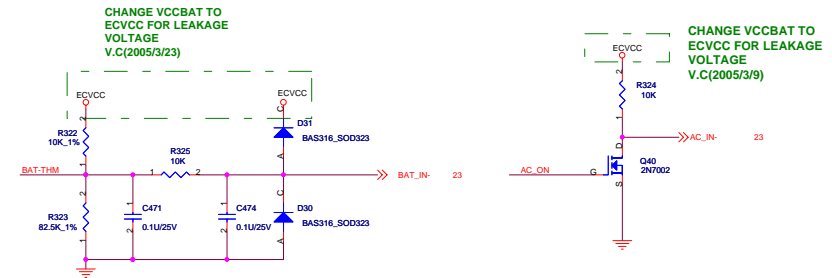
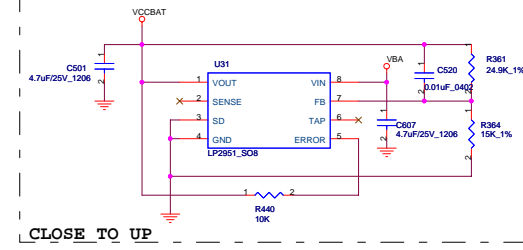
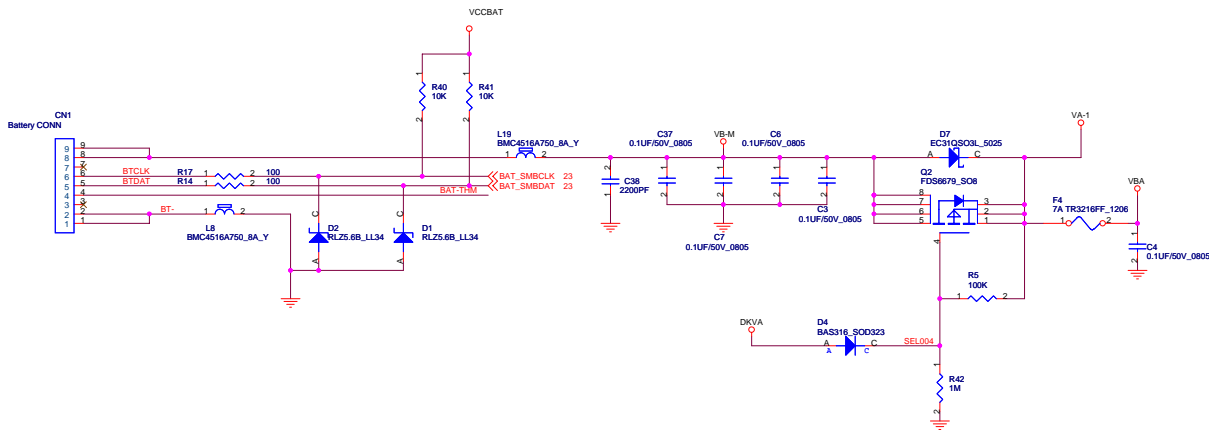
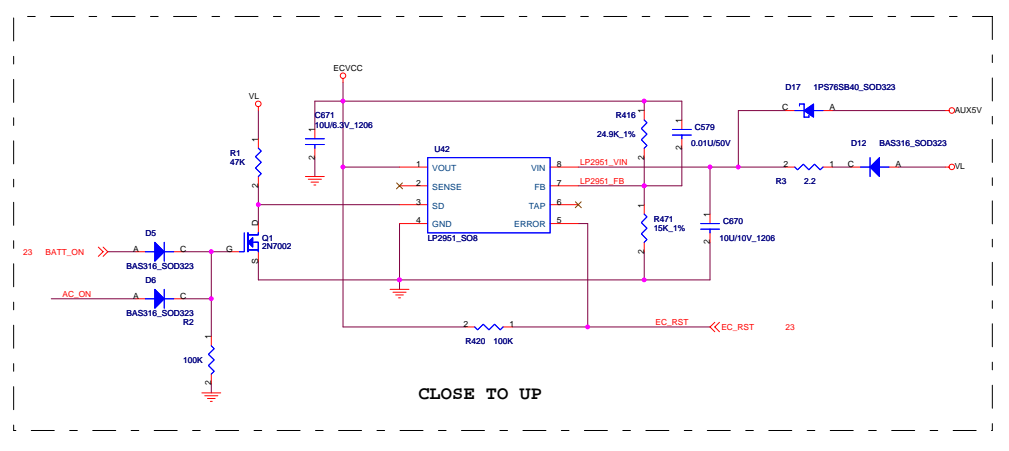
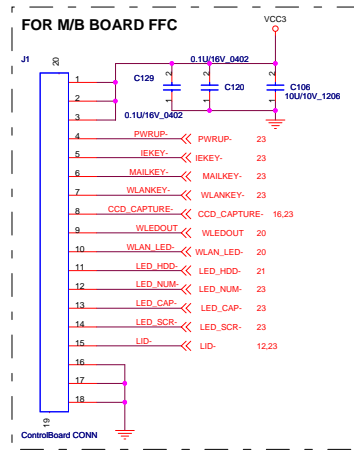
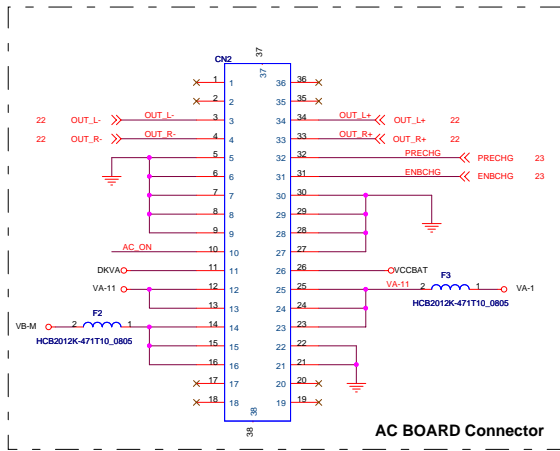
ECS Elitegroup Computer Systems

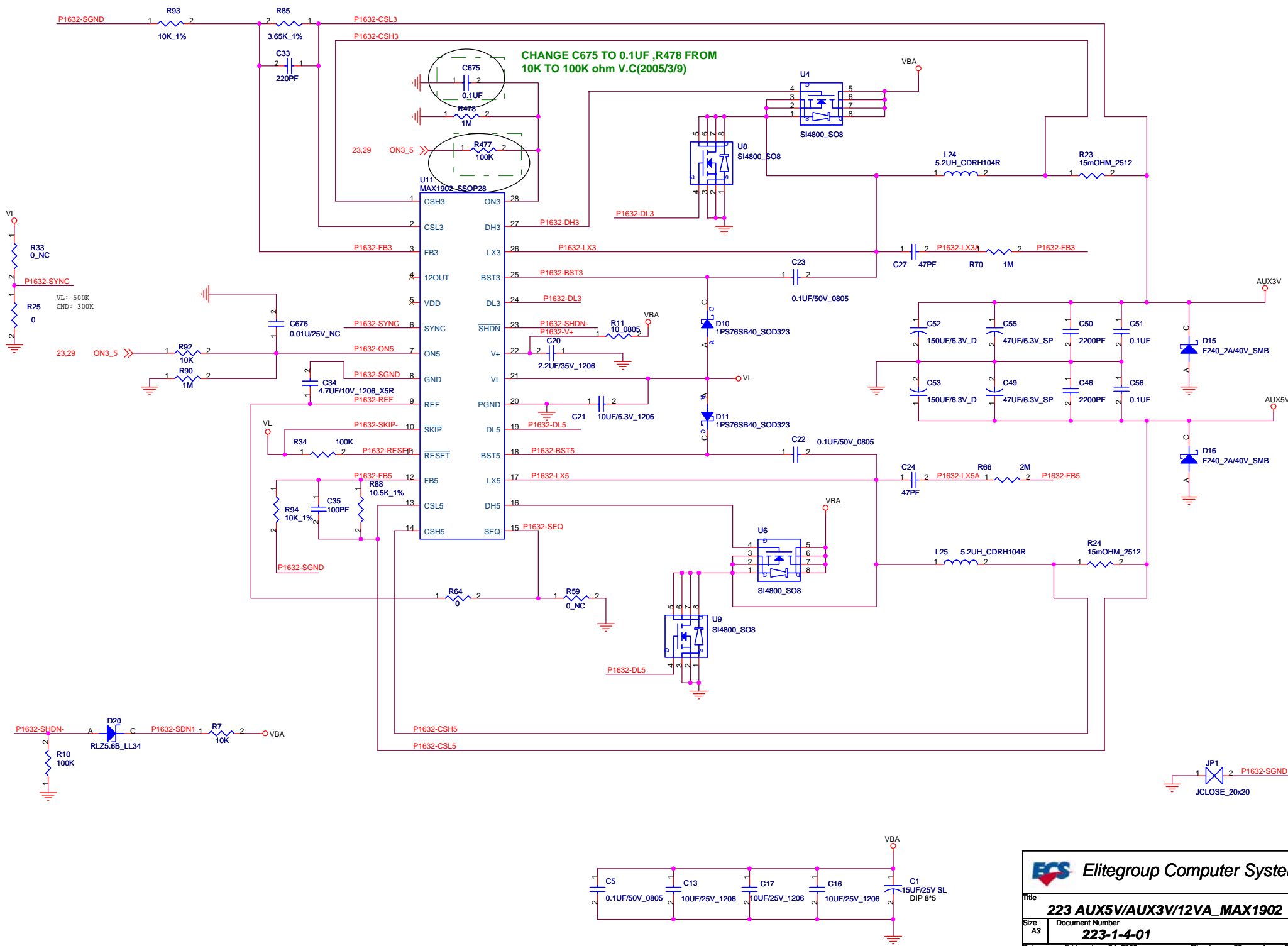
Title: **223 MINI PCI**

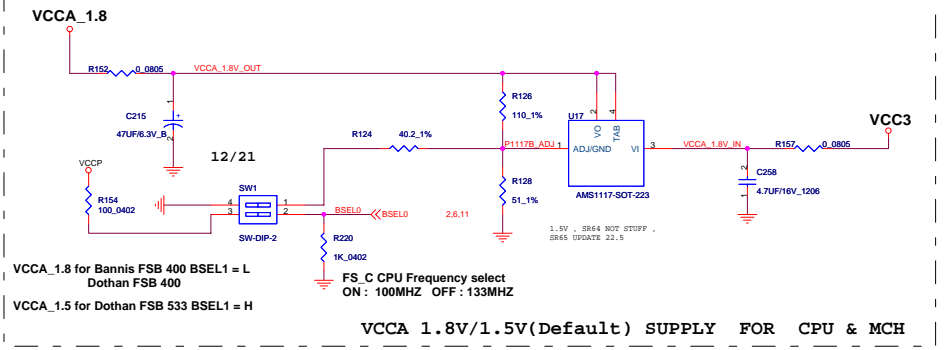
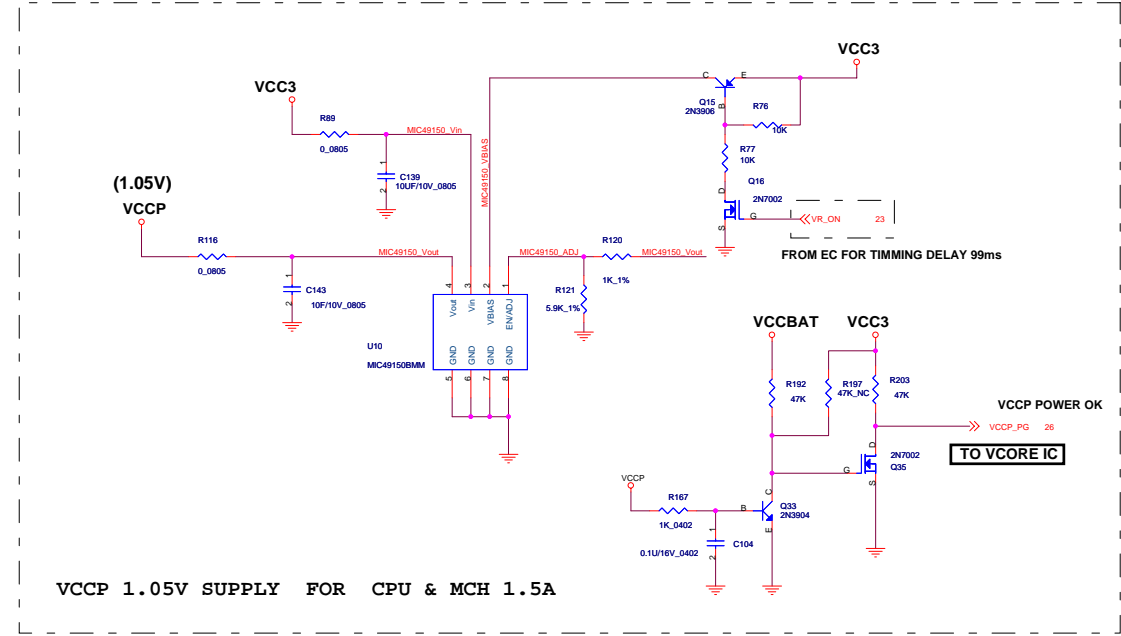
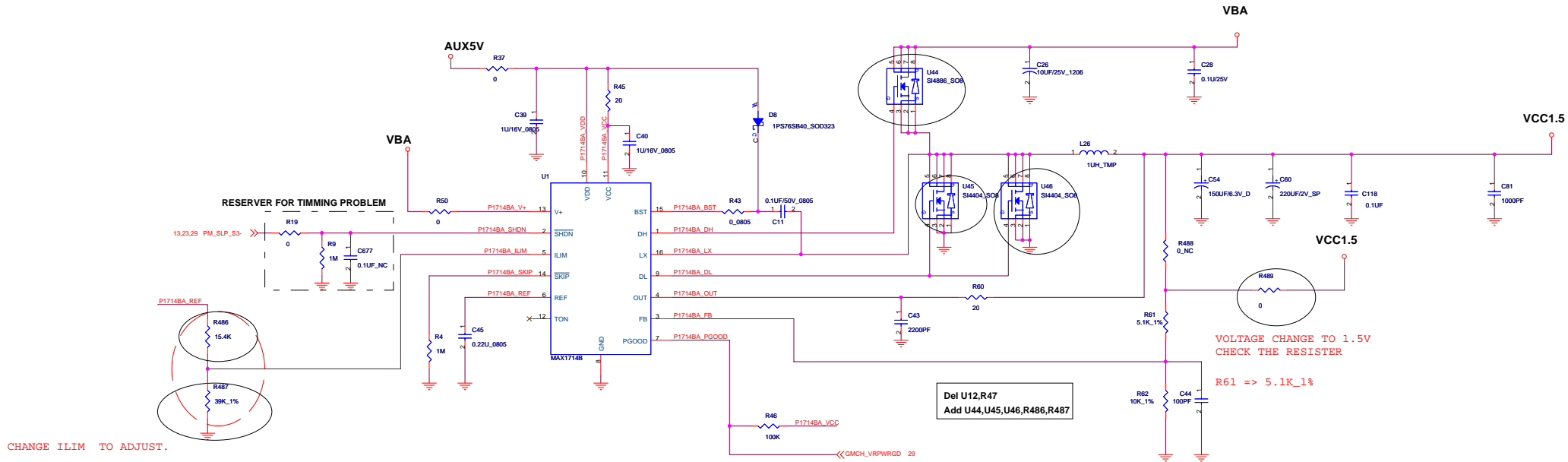
Size B Document Number: **223-1-4-01** Rev 1.0

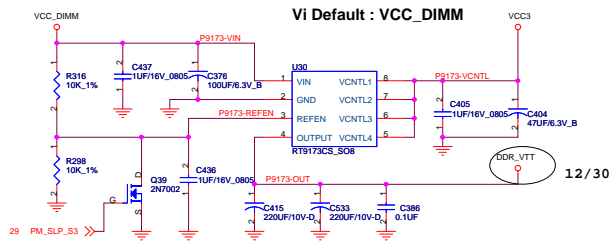
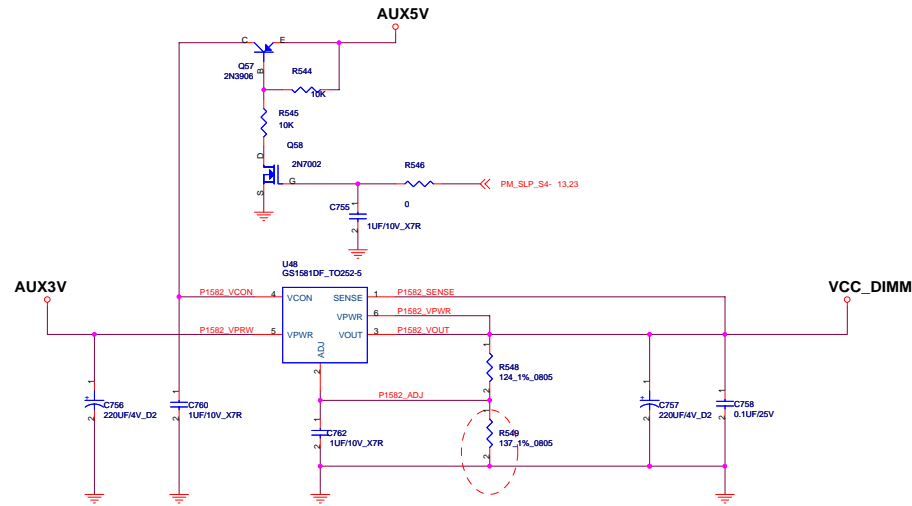
Date: Friday, June 24, 2005 Sheet 20 of 32



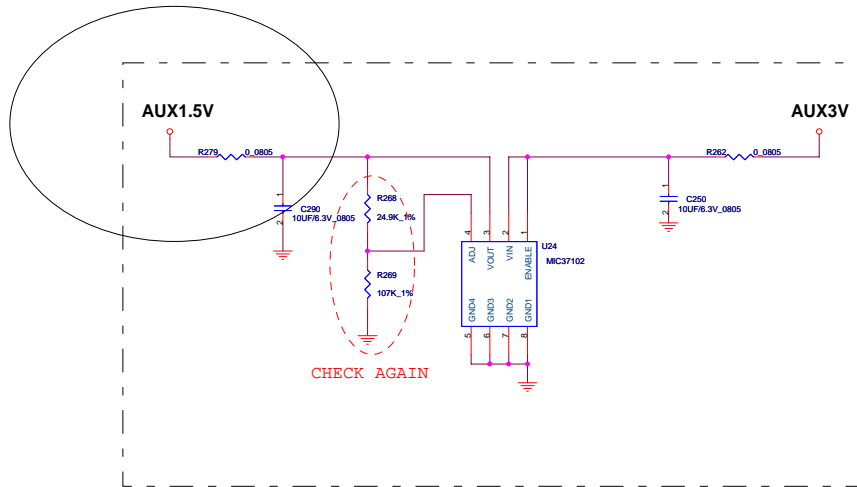


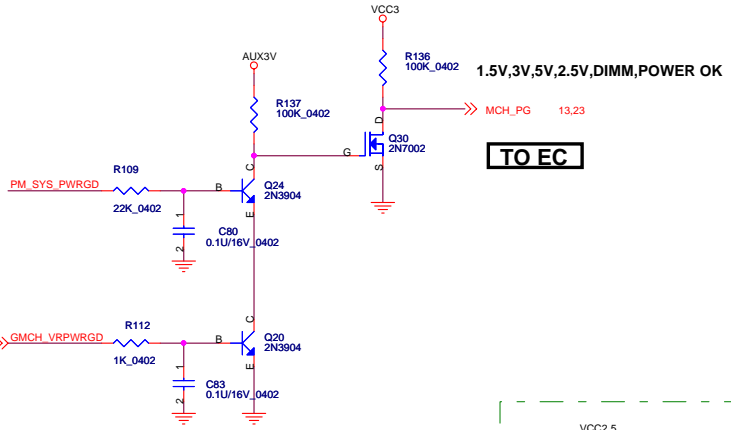
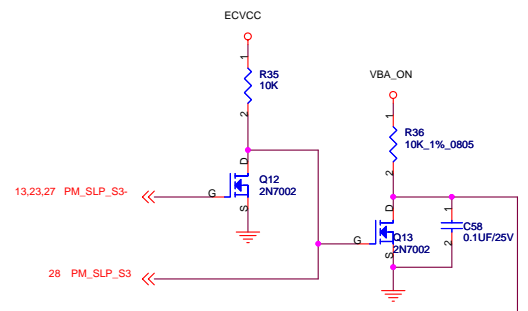
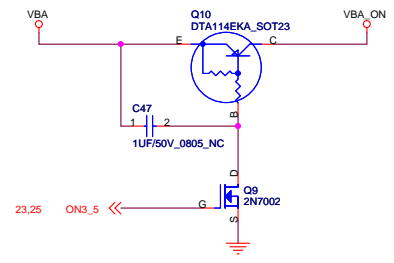
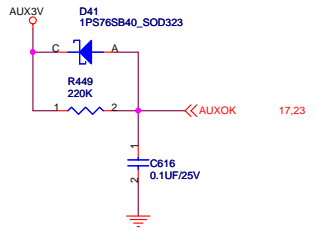






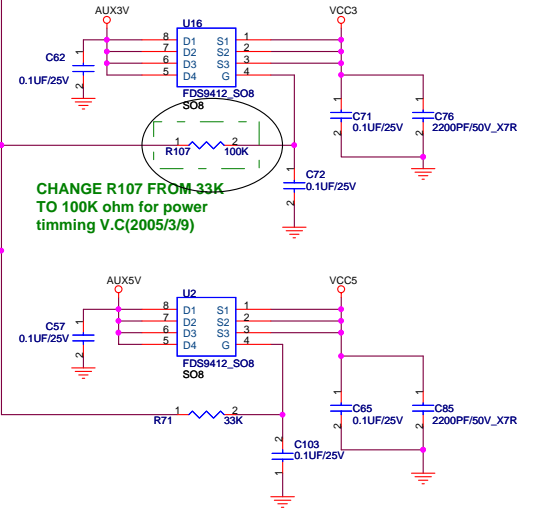
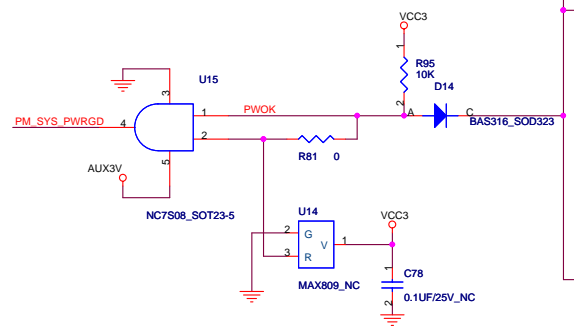
DIMM_2.5V SUPPLY 3.5A & VTT1.25V 1A FOR DDR



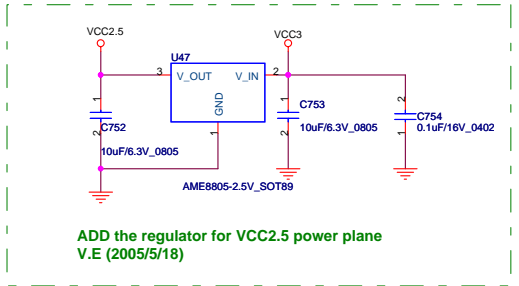


1.5V,3V,5V,2.5V,DIMM,POWER OK

TO EC

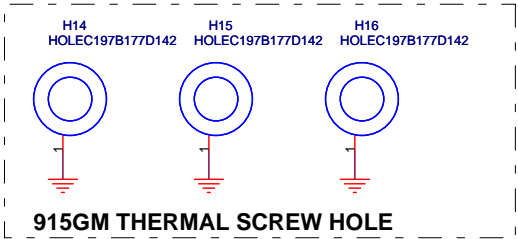
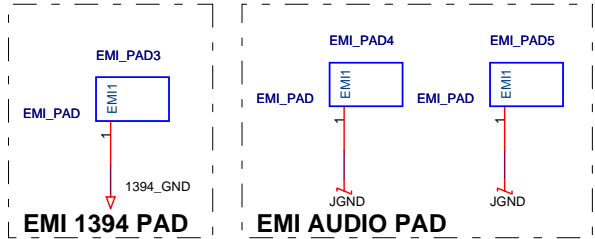
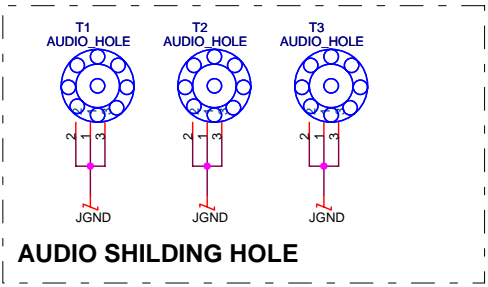
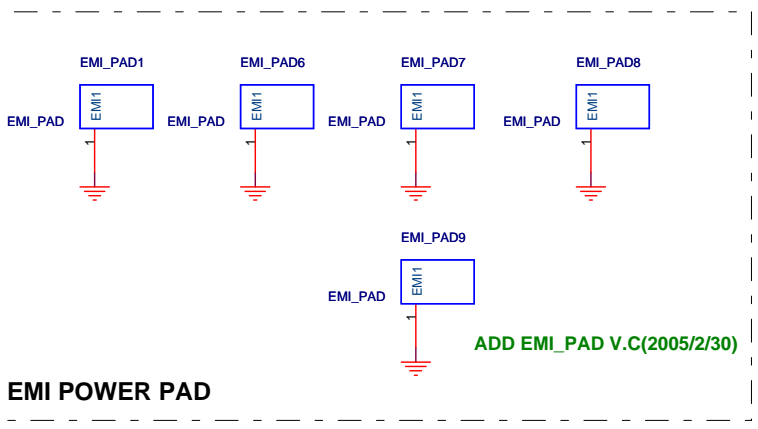
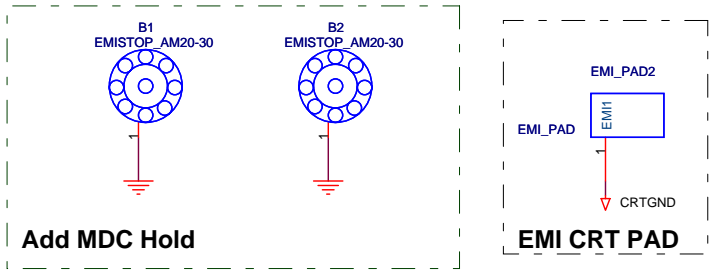
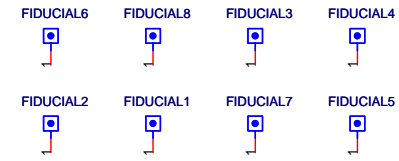
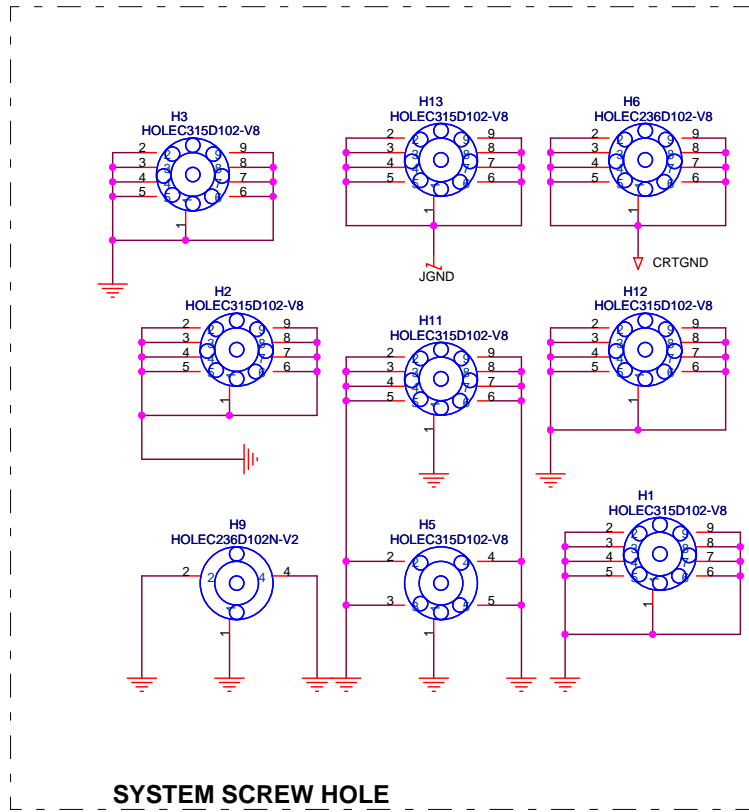
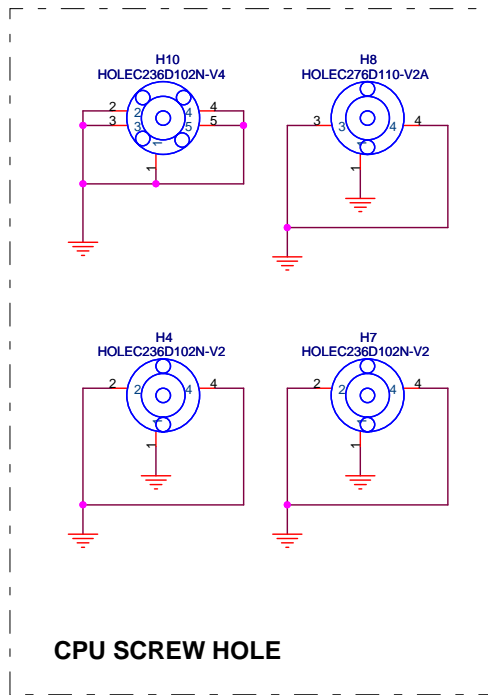


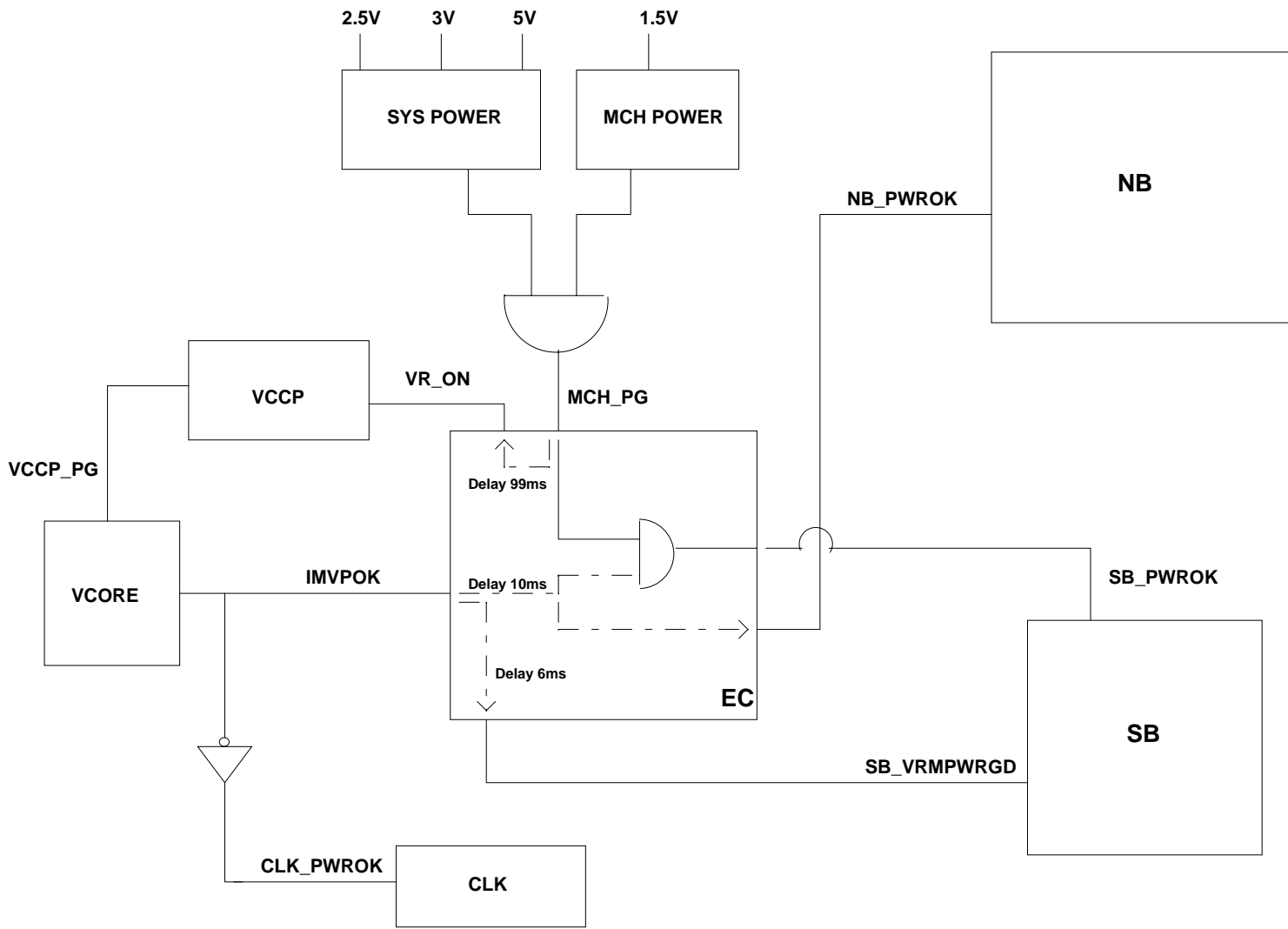
CHANGE R107 FROM 33K TO 100K ohm for power timing V.C(2005/3/9)



ADD the regulator for VCC2.5 power plane V.E (2005/5/18)

Title 223 POWER SW/VCC2.5		
Size	Document Number	Rev
Custom	223-1-4-01	1.0
Date:	Friday, June 24, 2005	Sheet 29 of 32





223 History List


A4 Stage V.A
1.Initial (2005/1/20)

- A4 Stage V.B
- 1.Change the DMI bus error TX-RX(2005/2/5)
 - 2.MODIFY SB_MUTE FROM GPI31 TO GPO19 (2005/2/15)
 - 3.MODIFY P_ID1 FROM GPI12 TO GPIO33 (2005/2/15)
 - 4.ADD R483 FOR PCI-EXPRESS WEAK (2005/2/15)
 - 5.CHANGR THE USB BUS FOR NET WRONG(2005/2/5)
 - 6.ADD 10K ohm for IMVPOK OC issue (2005/2/5)
 - 7.ADD R481 FOR INTERNAL REGULATOR 1.5V (2005/2/15)

A4 Stage V.C
1.Change the SB power net 3.3V_ICH(2005/3/7)

- A4 stage V.D
- 1.U27 from RTL8100 10/100 LAN change to BCM5789 for GIGA LAN.
 - 2.ADD R528,R529 33_1%_0402
R526,R527 49.9_1%_0402
C683,C684 0.1uF_0402
R533-R540 0_0402 FOR GIGA LAN.
 - 3.ADD R530 1K_0402 FOR PCIE_WAKE-.
 - 4.ADD R492,R426 NC FOR INTVRMEN REGULATOR DISABLE.
 - 5.ADD R132,R531 FOR VCC_DIMM CIRCUIT LIMIT-
V.D 050412
 - 6.ADD C274 47uF/6.3V_SP
FOR-V.D 050412

- A5 stage V1.0
- 1.Del Z3,Z4,Z5,Z7.
 - 2.R457,R464 from 20K change to 22K.
 - 3.SB GPIO[34] add test pad.

		
Title 223 HISTORY		
Size A3	Document Number 223-1-4-01	Rev 1.0
Date: Friday, June 24, 2005	Sheet 32	of 32